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TRANSMITTAL FORM (to be used for all correspondence after initial filing)			Application No.	09/517,705							
			Filing Date	March 2, 2000							
			First Named Inventor	Chunlin Liang							
			Group Art Unit	2811							
			Examiner Name	Steven Ho Yin Loke							
Total Number of F	Pages in This Submission	on 10	Attorney Docket Number	42390P5771D							
ENCLOSURES (check all that apply)											
Fee Transmittal	Form	Assignmen (for an App	t Papers lication)	After Allowance Communication to Group							
Fee Attact	hed	Drawing(s)		Appeal Communication to Board of Appeals and Interferences							
Amendment / Re	esponse	Licensing-r	elated Papers	Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)							
After Fina Affidavits/	ıl /declaration(s)	Petition		Proprietary Information							
Extension of Tim	Extension of Time Request		Convert a Application	Status Letter							
Express Abandonment Request		Power of A Change of	ttorney, Revocation Correspondence Address	Other Enclosure(s) (please identify below):							
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	SIGNATUR	E OF APPLICA	NT, ATTORNEY, OR AG	ENT							
Firm or	Raul D. Martin	nez, Reg. No.	46,904								
Individual name	BLAKELY, S	SOKOLOFF,	TAYLOR & ZAFN	MAN LLP							
Signature											
Date	April 28, 200	3									
CERTIFICATE OF MAILING/TRANSMISSION											
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231 on: April 28, 2003											
Typed or printed name Littian E. Rodriguez)											

Date

April 28, 2003

PTO/SB/17 (01-03)

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2811

42390P5771D

TRANSMITTAL for FY 2003 Complete if Known Application Number 09/517,705 Filing Date March 2, 2000 Effective 01/01/2003. Patent fees are subject to annual revision. First Named Inventor Chunlin Liang **Examiner Name** Applicant claims small entity status. See 37 CFR 1.27. Steven Ho Yin Loke

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TOTAL AMOUNT OF PAYMENT

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Group/Art Unit

Attorney Docket No.

METHOD OF PAYMENT (check one)	FEE CALCULATION (continued)								
☐ Check ☐ Credit card ☐ Money ☐ Other ☒ None	3. ADDITIONAL FEES								
Deposit Account	Large	Large Entity Small Entity							
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Charge any additional fee(s) required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.	1005	1,840 *		1,840 1	Requesting publication of SIR after Examiner action				
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to the above-identified deposit account	1251	110	2251	55	Extension for reply with	nin first month			
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1. BASIC FILING FEE	1253	930	2253	465	Extension for reply with	nin third month			
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Code (\$)	1255	1,970	2255	985	Extension for reply with	nin fifth month			
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1203 280 2203 140 Multiple Dependent claim, if not paid 1204 84 2204 42 **Reissue independent claims over original	1801	750	2801	375	Request for Continued	Examination (RCE	Ε)		
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**or number previously paid, if greater, For Reissues, see below	<u> </u>								
SUBMITTED BY	1 0	enistrati	on No			Comp	olete (if applica		
Name (Print/Type) Raul D. Martinez		Registration No. (Attorney/Agent)			46,904	Telephone (310) 207-3800			
Signature Raul D. Mat						Date	04/28	3/03	



Our Ref. No.: 42390P5771D

Examiner: Steven Ho Yin Loke

Art Unit: 2811

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Chunlin Liang, et al.

Application No.: 09/517,705

Filed: March 2, 2000

For: COMPLEMENTARY METAL GATE

ELECTRODE TECHNOLOGY

Box Non-Fee Amendment Assistant Commissioner for Patents Washington, D.C. 20231 RECEIVE NAY -6

AMENDMENT AND RESPONSE TO OFFICE ACTION

In response to the Office Action dated February 27, 2003, Applicants respectfully request entry of the amendments set forth below and consideration of the remarks that follow.

IN THE CLAIMS

Please substitute the following amended claims for the pending claims with the same numbers:

1. (Four Times Amended) A circuit device comprising:

a first transistor including a first metal gate electrode over a first gate dielectric on a first area of a semiconductor substrate and having a work function corresponding to the work function of one of P-type silicon and N-type silicon;

a second transistor complementary to the first transistor including a second metal gate electrode over a second gate dielectric on a second different area of a semiconductor substrate and having a work function corresponding to the work function of the other one of P-type silicon and N-type silicon; and

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